RD53A Emulator Status and Plans

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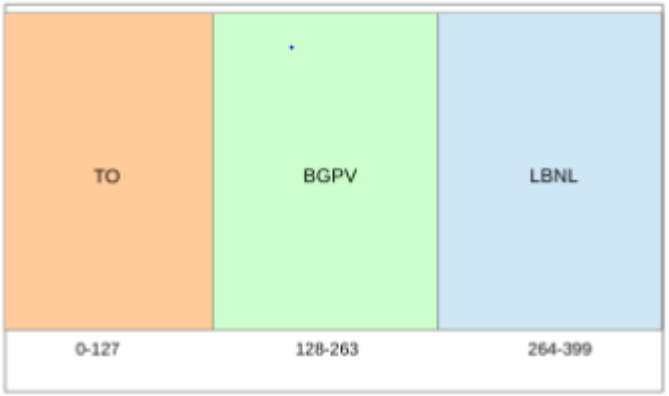
RD53A

- Development chip for HL-LHC
- Used to test 65 nm for ATLAS and CMS
  - Radiation tolerance
  - High data rate capability
- Multiple variations on analog front ends for comparison purposes
- Manufacture in October



Collaborators

- Joe Mayer began work on the emulator (graduated)
  - Thesis available: https://cds.cern.ch/record/2198312?ln=en

- Logan Adams – Graduate student
- Dustin Werran – Graduate student
- Douglas Smith – Undergraduate student
- Yangming Ke – Undergraduate student

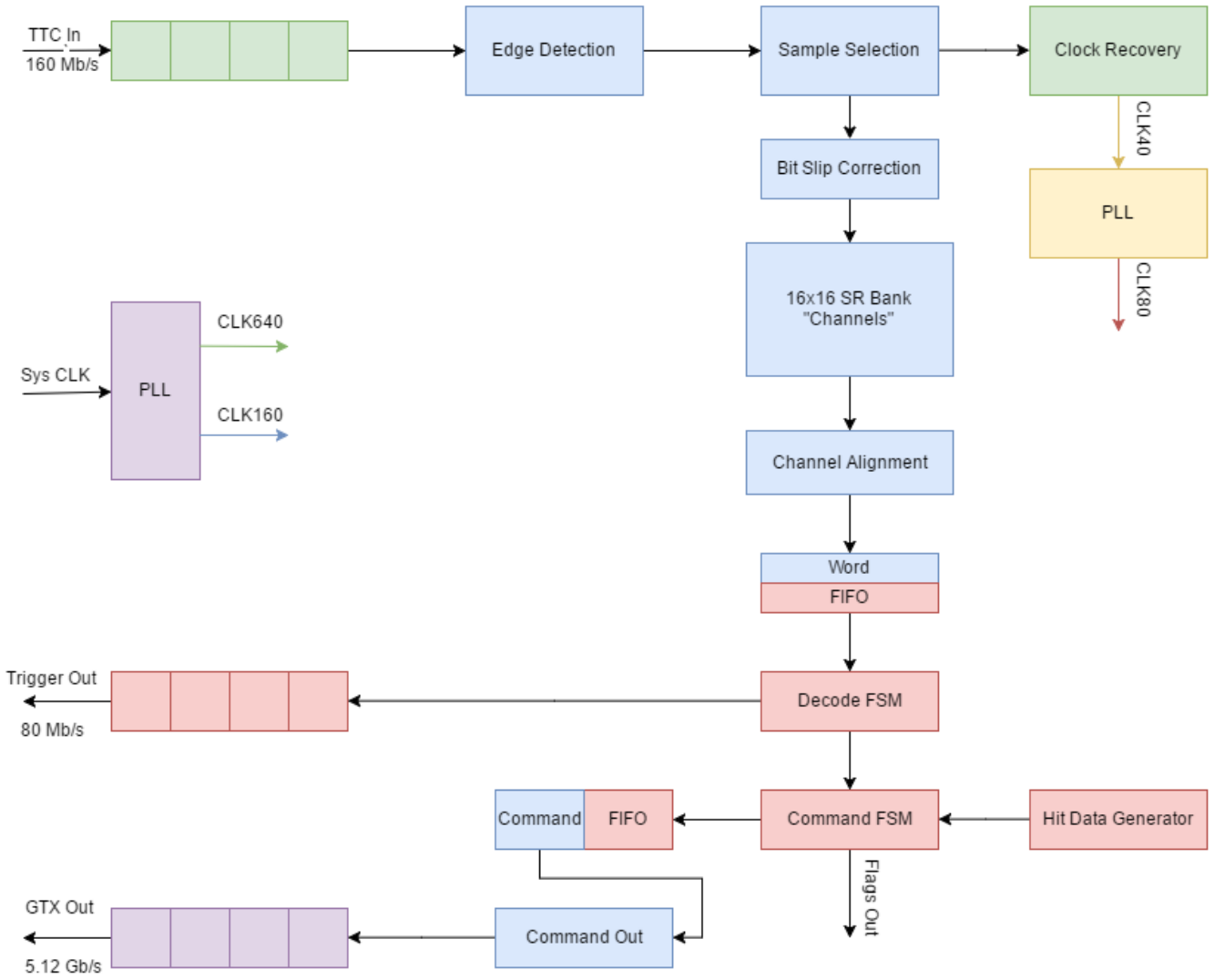
- Advised by
  - Shih-Chieh Hsu (UW Physics)
  - Scott Hauck (UW EE) – FPGA professor

- Working with Timon and Maurice and others to ensure emulator project is as useful to all as possible

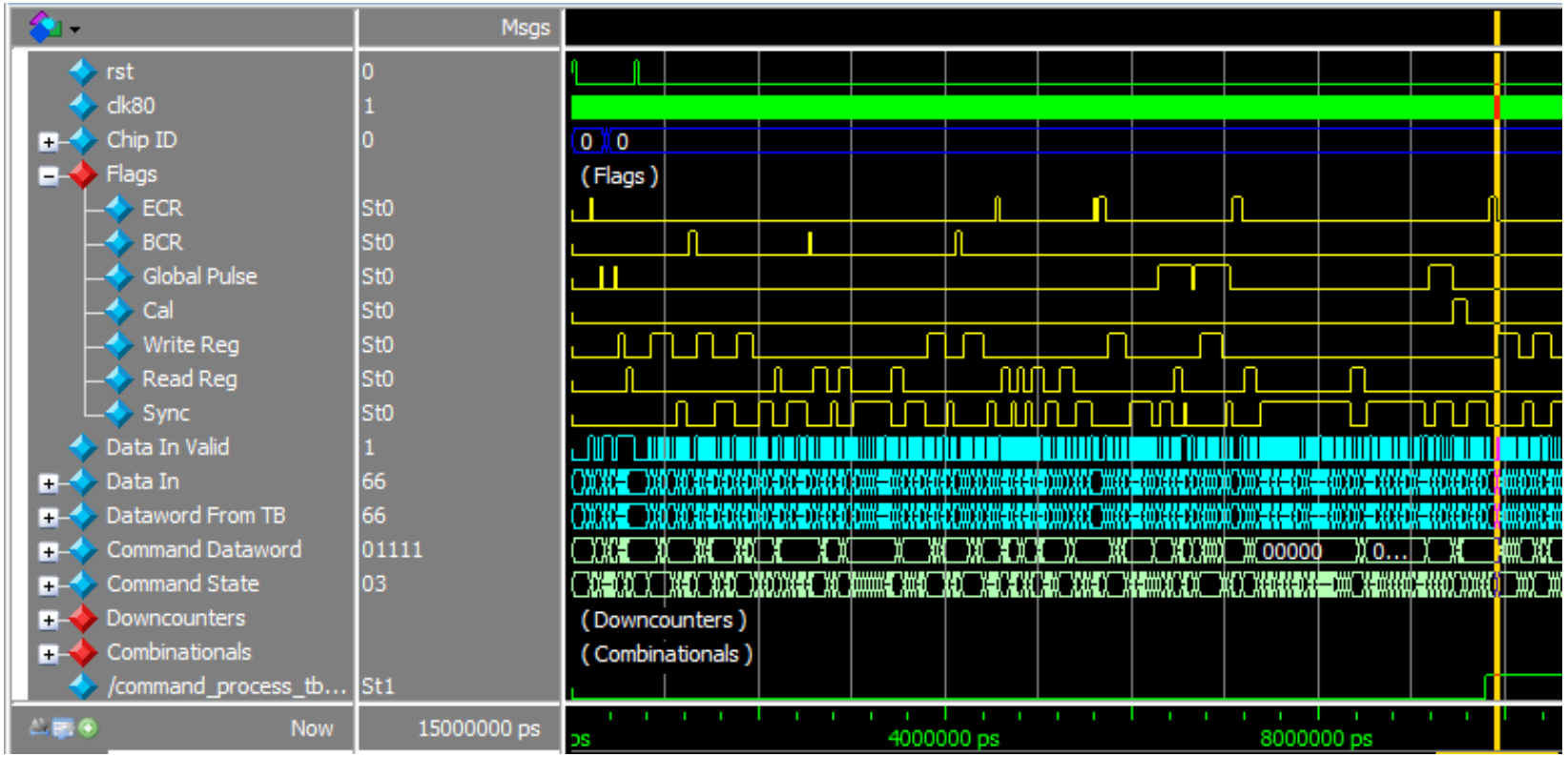
Current Implementation

- Simulation model of RD53A emulator working
  - Mostly up to specification
- “DAQ” system emulator
  - Test communication
  - Useful before real next-gen DAQ systems available
- Command module
  - Communicate between computer host and “DAQ”

Emulator Block Diagram

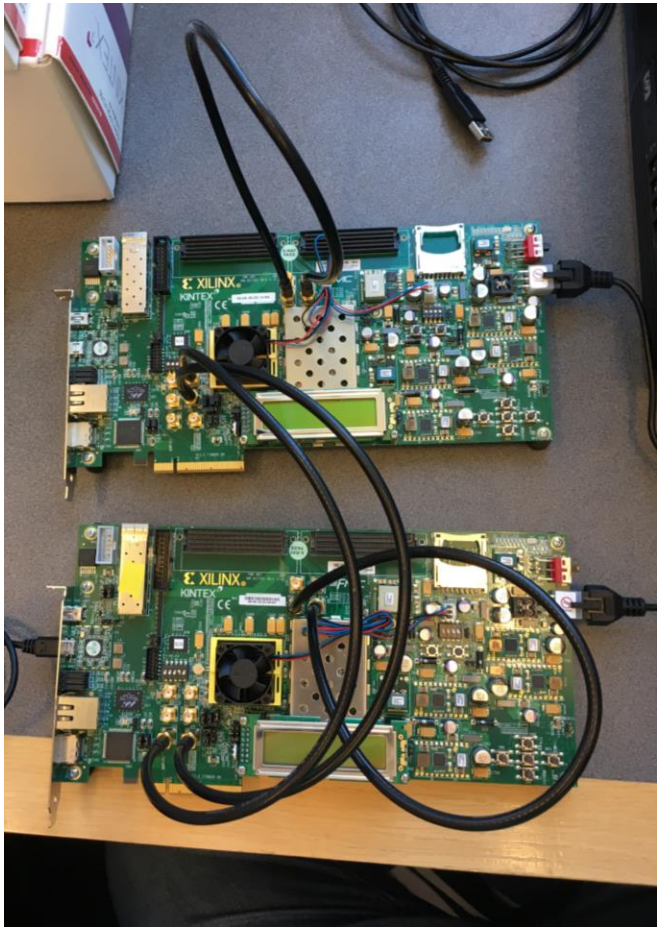


Command Process Wave



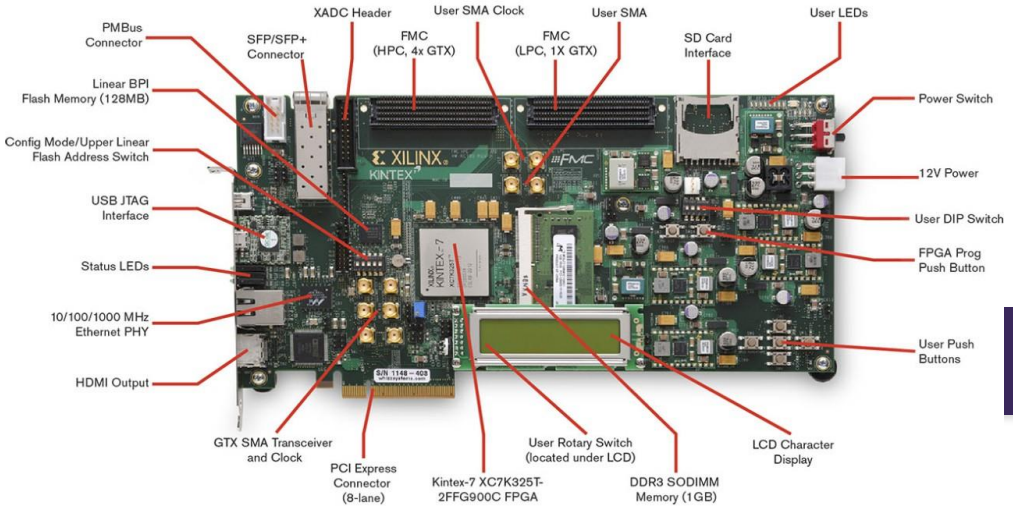
Current Testing

- Two Xilinx KC705 FPGA Development Boards
- Limited to SMA (available on the boards)
- DisplayPort testing when available



Development Plans

- Hit Data Emulation
- Global registers
- 5 Gig Links working on board
- Layout DisplayPort daughter card and spin
  - KC705 expansion
  - Possibly designed by OSU
- Testing with RCE as DAQ



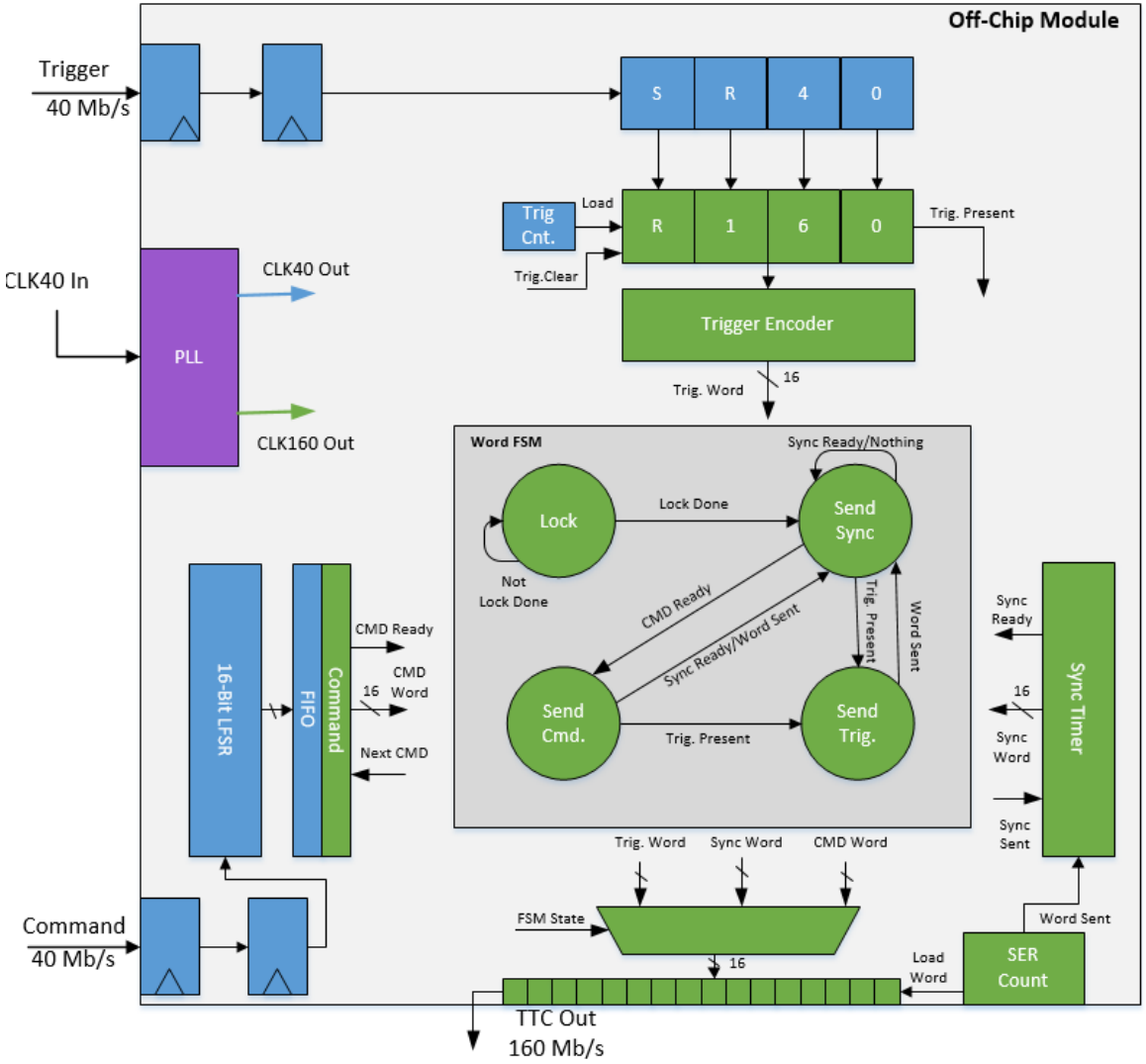
Feedback

- How can we make this as useful as possible?
  - What do you want to see implemented?
- Contact us if you are interested in the emulator.
  - All feedback on user experience is helpful.

Thanks!

Backup Slides

"DAQ" Diagram


Off-Chip Module
Trigger
40 Mb/s
S
R
4
0
Trig Cnt.
Load
R
1
6
0
Trig. Present
Trig.Clear
Trigger Encoder
Trig. Word
16
CLK40 In
PLL
CLK40 Out
CLK160 Out
Word FSM
Sync Ready/Nothing
Lock
Lock Done
Send Sync
Not Lock Done
CMD Ready
Sync Ready/Word Sent
Trig. Present
Word Sent
Send Cmd.
Trig. Present
Send Trig.
16-Bit LFSR
FIFO
Command
CMD Ready
CMD Word
16
Next CMD
Sync Ready
16
Sync Word
Sync Sent
Sync Timer
Trig. Word
Sync Word
CMD Word
FSM State
16
Word Sent
Load Word
SER Count
Command
40 Mb/s
TTC Out
160 Mb/s

System Test

- "DAQ-lite" designed to create/send TTC stream
- Testing system on KC705 FPGA with Host
- SMA Cables used for high speed communication (Not a system dependency)
- Capable of fully testing I/O and digital logic blocks
  - One-shot, continuous trigger, etc.